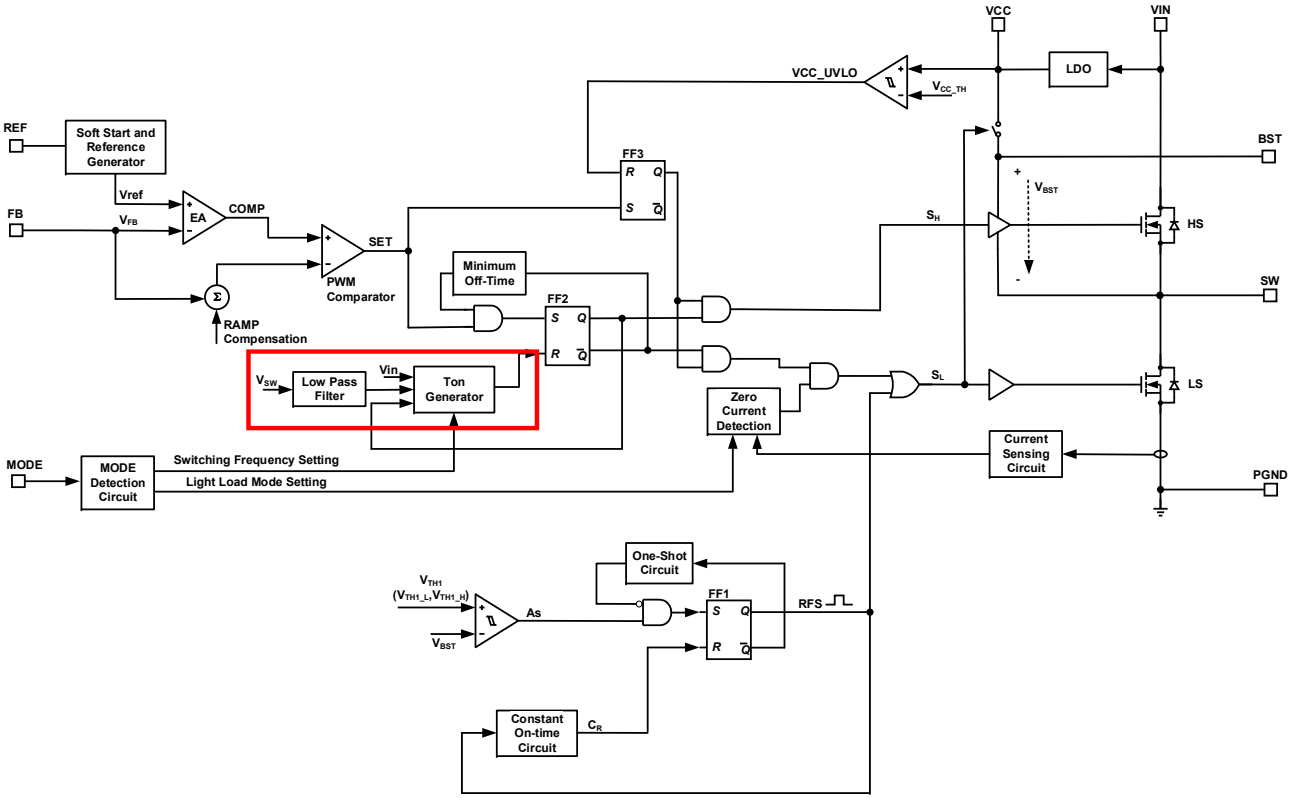
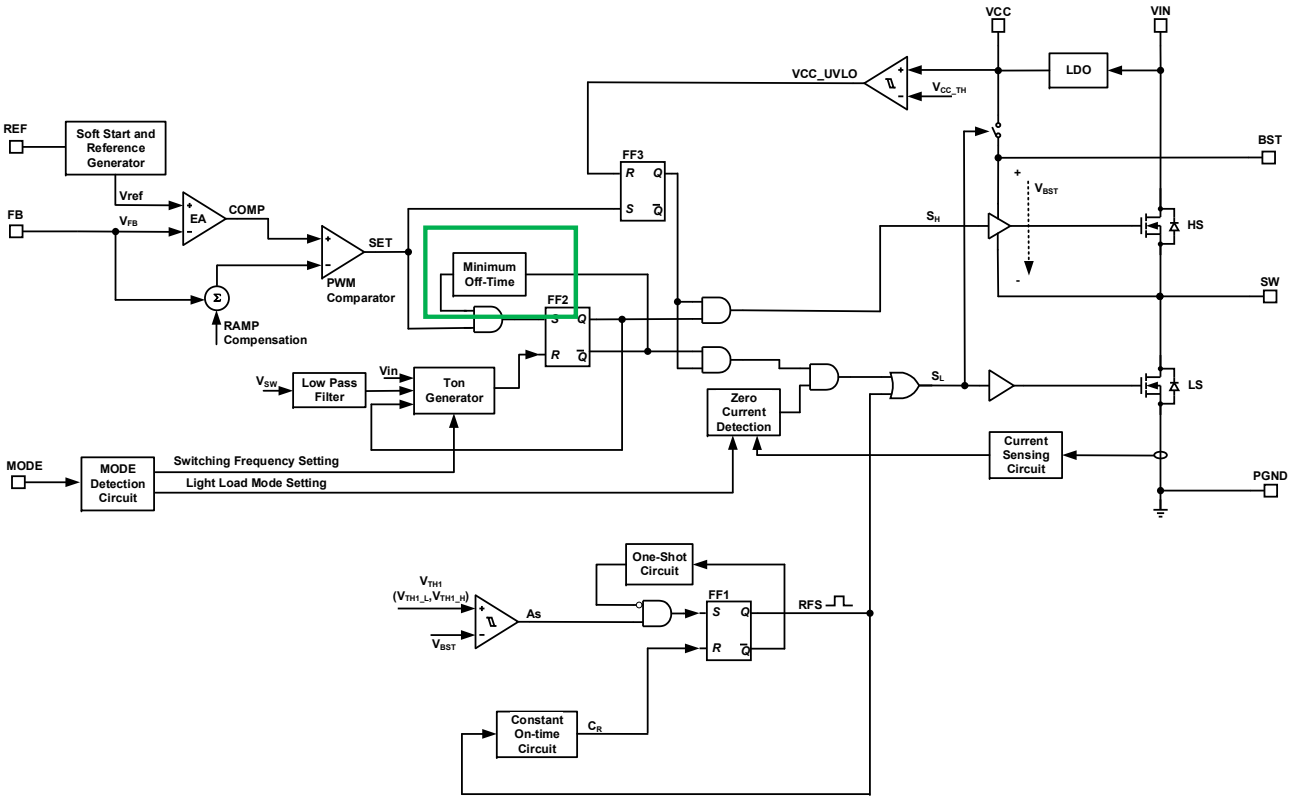
EXHIBIT 2

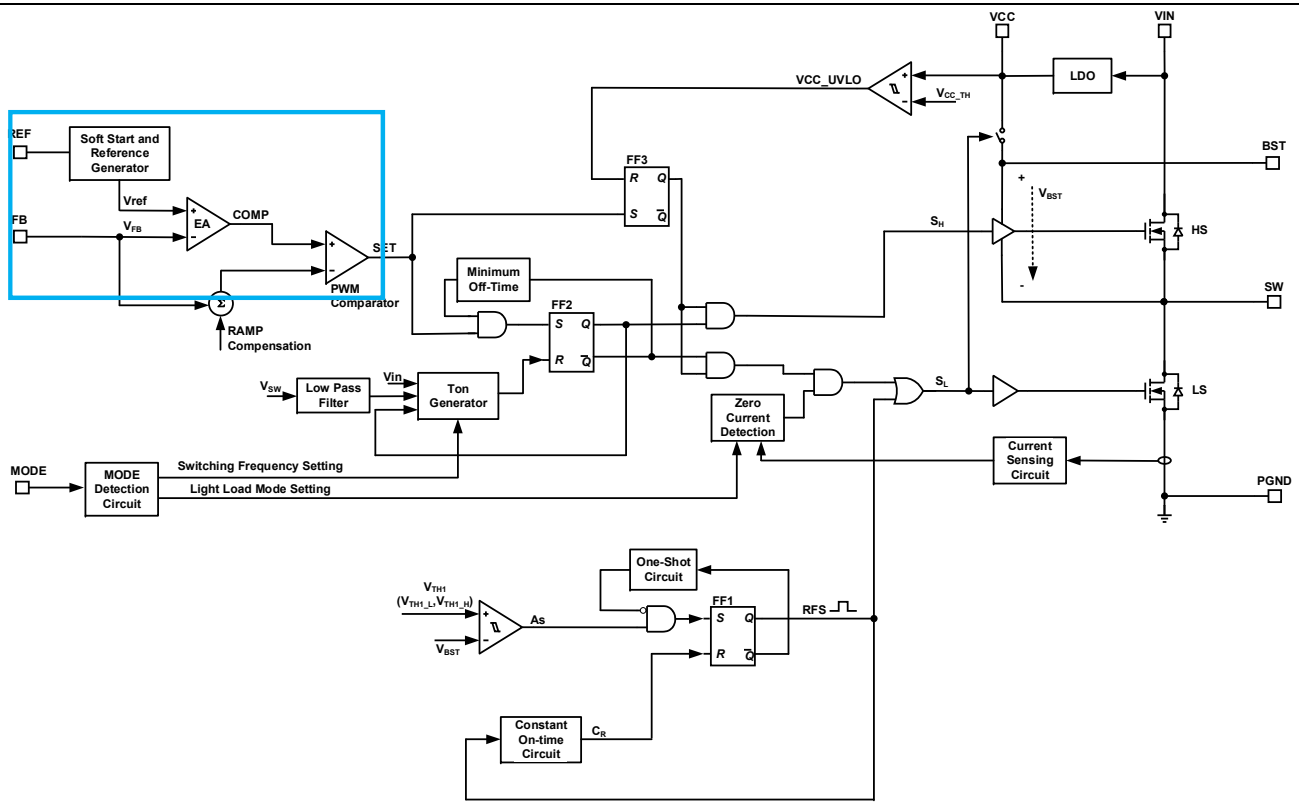
Infringement of Exemplary Claim 18 of U.S. Patent No. 9,041,377 (the '377 patent)

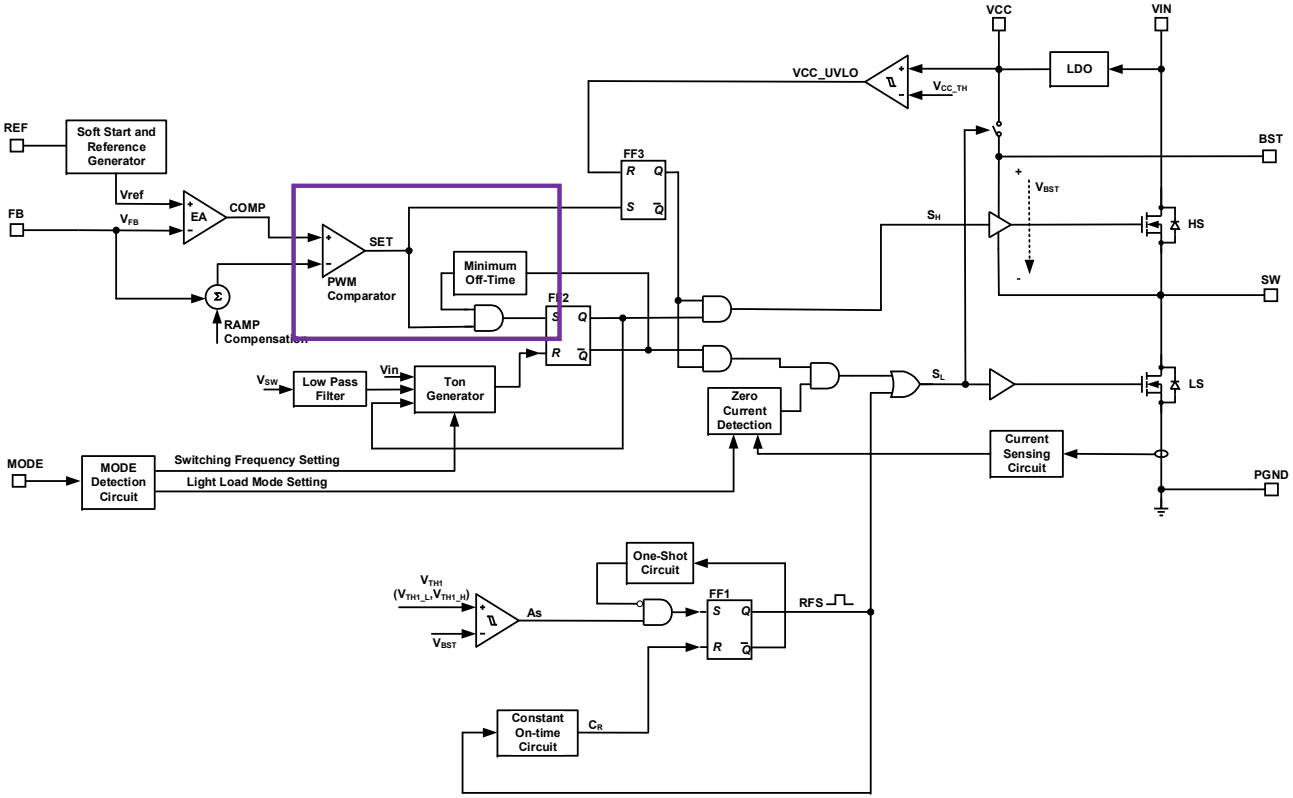
The accused products include, but are not limited to, Defendants' power module products, which include, but are not limited to at least the following models: RS53317, RS53318, RS53319, RS53328, and RS53355. (*See generally* datasheets for respective products) (describing bootstrap circuit technology for power converters.) A chart of exemplary claim 18 against exemplary RS53319 is provided below.

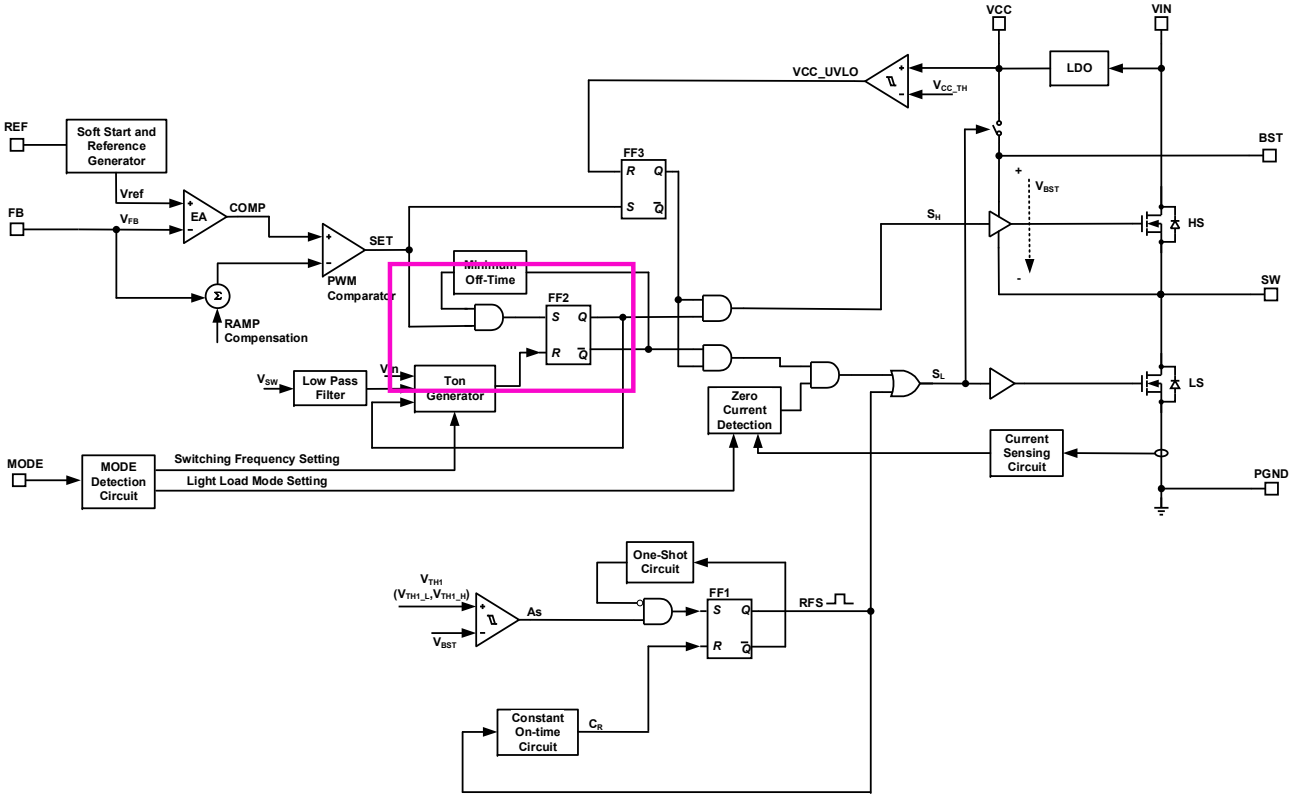
Annotations and identification of elements in this chart are preliminary, are not final, nor are they intended to limit Plaintiff's identification of claim elements in Reed's infringing products. Furthermore, RS53319 and claim 18 have been provided as representative, and Plaintiff reserves the right to identify additional products and claims, and identify further representative products. Plaintiff reserves the right to amend, supplement, expand, modify, or narrow its identifications in the accused products as it develops facts during discovery, based on the Court's claim constructions, or for any other allowable purpose in this action.

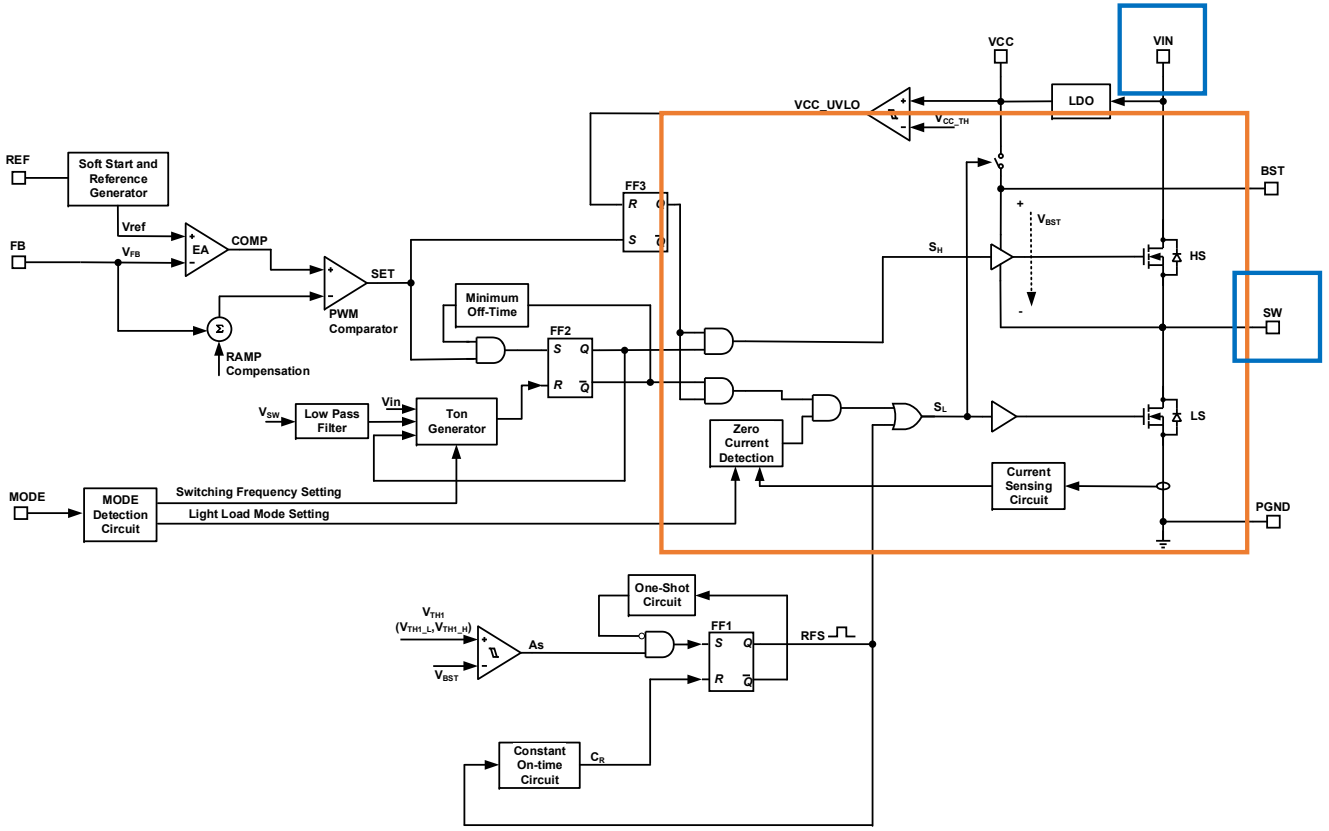
9,041,377	RS53319
18. A step-down regulator, comprising:	The RS53319 is a controller for a power converter. (*See generally* RS53319 Datasheet.)
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;	The RS53319 has an "on-time generator" generating an on-time signal, based on the switching signal (V_{SW}) and the control signal, as annotated in red below.  RS53319 Reverse Engineering Schematic
a minimum off time generator configured to	RS53319 has a minimum off time generator that generates a minimum off time signal in accordance with the control signal it receives, as annotated in green below.

receive the control signal, and to generate a minimum off time signal in accordance with the control signal;	 RS53319 Reverse Engineering Schematic
a comparator configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to receive a	RS53319 has a comparator configured to receive a feedback signal (V_{FB}) and a reference signal (V_{ref}), as annotated below in blue. Comparator generates a comparison signal based on V_{FB} and V_{ref}.

reference signal, and wherein based on the feedback signal and the reference signal, the comparator generates a comparison signal;	 RS53319 Reverse Engineering Schematic
an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal,	RS53319 has an *and-gate* coupled to the (1) comparator and (2) minimum off time generator to receive the (1) comparison signal and (2) minimum off time signal, as annotated below in purple. In RS53319, the *and-gate* generates an output signal based on the comparison signal and the minimum off time signal.

wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal;	 RS53319 Reverse Engineering Schematic
a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is	RS53319 has a flip-flop (annotated below in pink) having a set and reset terminal (i.e. set-reset latch). The flip-flop also has an output. The reset terminal of the flip-flop is coupled to the “on-time” generator.

coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and	The set terminal of the flip-flop is coupled to the *and-gate*, receiving the output signal of the *and-gate*. The flip-flop generates the control signal based on the on-time signal and the output signal.  RS53319 Reverse Engineering Schematic

a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.	RS53319 has a "power stage", annotated in orange below. The "power stage" is coupled to the output terminal of the flip-flop, where the "power stage" receives the control signal. The "power state" converts the input voltage (V_{IN}) into the switching signal (V_{SW}) based on the control signal, as annotated in dark blue below.  RS53319 Reverse Engineering Schematic